REMARKS

This amendment accompanies a Request for Continued Examination filed in connection with the referenced application.

Claims 1-13, 17, and 18 were pending. Claims 1-3, 5-9, 11-13, and 17 have been amended. Claims 19-22 have been added. Claims 1-13 and 17-22 are pending.

Claim 1-12, 14, 17 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,886,353 to Spivey et al., in view of U.S. Pat. No. 5,510,623 to Sayag et al., further in view of U.S. Pat No. 5,937,027 to Thevenin et al., U.S. Pat. No. 6,396,539 to Heller et al., and Examiner's official notice (deemed "admitted prior art" by the Examiner). This rejection respectfully is traversed.

The present invention as recited in amended claim 1 is a CMOS image sensor circuit having "a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and a control portion with image sensor logic on said substrate." The image sensor logic is "electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually," and chip logic is "associated with parts of said image sensor portion other than said rows individually." The image sensor portion has "a first area and a second area." The image sensor substrate is "formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges." The "second set of parallel edges" includes "a third edge and a fourth edge." The image sensor substrate extends "between said first edge, said second edge, and said third edge, such that said first area of said image sensor portion is adjacent said first edge and said third edge of said image sensor substrate and said second area of said image sensor portion is adjacent said second edge and said third edge of said image sensor substrate." The row logic is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion." A "pixel interpolator and said chip driver circuitry" are "located between said first area and

said second area of said image sensor portion and said fourth edge of said image sensor substrate." A second CMOS image sensor substrate is "configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate."

The reference to Spivey et al. discloses a large-format array having readout circuitry located at edges of the array. The location is based on a "Circuit Defect Strategy" for the large format array in which the sensor area is divided into two regions of differing nature. One region is the very large area occupied by the pixel array 183. The other region is the very small area occupied by the readout circuits 133 and 186 at the edges of the array. See Fig. 15A and col. 10, lines 26-54. By locating the readout circuitry at the edges of the array according to the circuit defect strategy, the Spivey et al. reference overcomes problems of low CMOS process yield, and achieves the object of providing a large-scale sensor.

The Examiner also has pointed to the alternative disclosure in the Spivey et al. reference described at col. 26, lines 33-52, in which readout circuitry is integrated with the pixel array. According to the Spivey et al. reference, in this alternative image sensor, there is "pixel (readout) circuitry in each pixel." Consequently, rather than teaching or suggesting the invention of claim 1, Spivey et al. teaches directly away from a CMOS image sensor having "a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and a control portion with image sensor logic on said substrate," "said *image sensor portion* having a first area and a second area." This is particularly so since Spivey et al. teaches that the image is divided into two "differing" regions, one for the image array and one for the control circuitry. Further, the Spivey et al reference does not teach or suggest that row logic is "physically located inside said image sensor portion *in place of* a plurality of pixels of the array forming said image sensor portion." Spivey et al. does not anticipate or render obvious the invention recited in claim 1.

Claim 1, and its dependent claims 2-7 and 19-21, are submitted as patentable over the cited reference to Spivey et al.

The reference to Sayag et al. does not cure the deficiencies of the Spivey et al. reference. Sayag et al. discloses an image sensor having all of its readout circuitry located in the center of the imager array as part of a photosensitive read-out register. As noted above, the reference to Spivey et al. discloses strategies for forming a large-scale format sensor in which a large image array region is provided with readout circuitry located either on the edges of the array, or within each pixel of the array. There is no motivation in the cited prior art references to modify the Spivey et al. reference by dividing the large image array region into two areas using centrally-located readout circuitry. The proposed modification would be contrary to the design principles of the Spivey et al. reference, and thus the teachings of the Spivey et al. and Sayag et al. references are not sufficient to render obvious claim 1 and its dependent claims 2-7.

The reference to Thevenin et al. does not cure the deficiencies of Spivey et al. and Sayag et al. The Thevenin et al. reference discloses an image sensor that has readout circuitry located *underneath* the pixel array, and thus teaches away from putting the logic on or *in place of* pixels in the array. Thevenin et al. does not provide the missing motivation for modifying the Spivey et al. reference as would be required to arrive at the present invention.

The reference to Heller et al. does not cure the deficiencies of the references to Spivey et al., Sayag et al., and Thevenin et al. The Heller et al. reference has been cited as providing on-chip interpolation circuitry. Heller et al. discloses an image sensor having an array 12 and readout circuitry located separately on a substrate 10. Heller et al. does not supply the necessary motivation to modify Spivey et al. in the manner suggested by the Examiner.

The Examiner has taken official notice that it is desirable to make edges as small as possible in order to increase image sensitivity in image sensors. The Examiner's official

notice does not provide the motivation to modify Spivey et al. based on the Sayag et al. reference.

Claims 1-7 are submitted as patentable over the cited references to Spivey et al., Sayag et al., Thevenin et al., and Heller et al., and the Examiner's official notice.

Claim 8 recites a "method of operating a large format image sensor" by "first obtaining an image sensor chip which has first and second edges where said image sensor comes within two pixel pitches of said first and second edges, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor, and an image portion divided into two areas." The method includes "abutting said image sensor chip against a similar image sensor chip of corresponding construction," and "interpolating missing pixels caused by both said row select logic and by spaces between said image sensor chips."

The reference to Spivey et al. discloses operating a large-format image sensor which includes a large imager array region and control portions located on the edges of the imager array, or having pixel readout circuitry integrated into each of the pixels of the array. Spivey et al. does not teach or suggest, but rather teaches away from, "operating a large format image sensor" by "first obtaining an image sensor chip" which has "a control portion with row selecting logic in place of a plurality of central pixels of the image sensor, and an image portion divided into two areas." Consequently, Spivey et al. does not teach or suggest operating an image sensor by "abutting said image sensor chip against a similar image sensor chip of corresponding construction," and "interpolating missing pixels caused by both said row select logic and by spaces between said image sensor chips."

Claim 8 is not anticipated or rendered obvious by the reference to Spivey et al.

The reference to Sayag et al. does not cure the deficiencies of the Spivey et al. reference. The Sayag et al. reference discloses operating an imager array that is divided centrally by a photosensitive read-out register. The Examiner's proposed modification of the structure disclosed by the Spivey et al. reference based on Sayag et al. would be

contrary to the circuit defect strategy, a basic principle of the design proposed by the Spivey et al. reference. The proposed combination does not render claim 8 *prima facie* obvious.

The reference to Thevenin et al. does not cure the deficiencies of Spivey et al. and Sayag et al. The Thevenin et al. reference teaches placing control circuitry underneath a pixel array, and can not provide the missing motivation to modify the device taught Spivey et al. based on the disclosure of the Sayag et al. reference.

The reference to Heller et al. does not cure the deficiencies of Spivey et al., Sayag et al., and Thevenin et al. The image sensor disclosed by the Heller et al. reference has control circuitry that is completely separate from the imager array. The Heller et al. reference can contain no motivation to modify the Spivey et al. reference as suggested by the Examiner based on the Sayag et al. reference.

The Examiner's official notice does not cure the deficiencies of Spivey et al, Sayag et al., Thevenin et al., and Heller et al. The Examiner's official notice relates to on-chip interpolation, and not to anything that suggests modifying the Spivey et al. reference based on Sayag et al. Claim 8 is submitted as patentable over the cited references to Spivey et al., Sayag et al., Thevenin et al, and Heller et al., and the Examiner's official notice.

Claim 9 recites a CMOS imager having "a first CMOS image sensor having an image sensor portion arranged in an array of rows and columns, said first CMOS image sensor formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge." The first CMOS image sensor has "a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said CMOS image sensor portion and thereby forming at least two image sensor areas." The control portion includes "a pixel interpolator located between said at least two image sensor areas and one of said edges of said first CMOS image sensor."

Spivey et al. discloses CMOS imager having a large image array region and a small control region. The control region is located either on the edges of the large image array, or integrated into each of the image array pixels as part of a design strategy used to obtain large pixel arrays with few critical defects. The Spivey et al. reference teaches away from a CMOS imager with a first CMOS image sensor having "a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said CMOS image sensor portion and thereby forming at least two image sensor areas." The Examiner proposes to modify the imager disclosed by Spivey et al. based on Sayag et al. Sayag et al. discloses an imager with a central, photosensitive read-out register. Modifying the reference to Spivey et al. based on the Sayag et al. reference would be counter to the design strategy of the Spivey et al. reference. Spivey et al. and Sayag et al. do not render claim 9 obvious. Neither the references to Thevenin et al. and Heller et al., nor the Examiner's official notice, taken alone or in combination, can provide the missing motivation to change the design principle of Spivey et al. based on Sayag et al. Thevenin et al. teaches locating readout circuitry underneath the pixel array, and Heller et al. teaches readout circuitry completely separate from the imager array. The Examiner's official notice relates to manufacture of thin edges, and does not provide motivation to modify the teachings of Spivey et al. based on Sayag et al.

Claim 9, and its dependent claim 10, are submitted as patentable over the references to Spivey et al., Sayag et al., Thevenin et al., and Heller et al., and the Examiner's official notice.

Claim 11 recites a method of fabricating a CMOS imager. The method includes "fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, each of said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge, said at least two image sensors having a control portion and a centralized row-local control portion, said centralized row-

local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor and thereby forming at least two image sensor areas for each of said at least two CMOS image sensors, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said image sensor." The "at least two CMOS image sensors" are abutted together, and the "control portions of said at least two CMOS image sensors" are integrated "such that said at least two CMOS image sensors function as a single CMOS imager."

The reference to Spivey et al. discloses a method of fabricating an image sensor in which defects are minimized by having a large image array region and a small control region. The control region is located on edges of the large image array region, or is integrated into each pixel of the array. The reference to Spivey et al. teaches away from a method of fabricating a CMOS imager having at least two CMOS image sensors, each CMOS image sensor "having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor and thereby forming at least two image sensor areas for each of said at least two CMOS image sensors."

The reference to Sayag et al. does not cure the deficiencies of Spivey et al. The imager disclosed in the Sayag et al. reference features a photosensitive read-out register located centrally on the imager array. The Examiner's proposed modification of the Spivey et al. reference based on the Sayag et al. reference requires reconstructing the device disclosed by the reference to Spivey et al. in a manner contrary to the design considerations of the Spivey et al. reference. Claim 11 is not rendered prima facie obvious by the references to Spivey et al. and Sayag et al.

The references to Thevenin et al. and Heller et al., and the Examiner's official notice, do not cure the deficiencies of Spivey et al. and Sayag et al. Thevenin et al. teaches readout circuitry located underneath the pixel array, and Heller et al. teaches readout circuitry completely separate from the imager array. The Examiner's official notice relates

to providing thin edges in imaging devices, and does not provide motivation to modify the teachings of Spivey et al. based on Sayag et al.

Claim 11, and its dependent claim 12, are submitted as patentable over the references to Spivey et al., Sayag et al., Thevenin et al., and Heller et al., and the Examiner's official notice.

Claim 17 recites a method of fabricating a CMOS imager that includes "fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, each of said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, said a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge, each of said at least two image sensors having a control portion and a centralized row-local control portion." The "centralized row-local control portion" is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor," and thereby forms "at least two image sensor areas in each of said at least two CMOS image sensors, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said image sensor."

The reference to Spivey et al. discloses fabricating a CMOS image sensor which has a large image sensor portion and a small control portion. Spivey et al. teaches away from making a CMOS image sensor having a "centralized row-local control portion" that is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor," and thereby forms "at least two image sensor areas in each of said at least two CMOS image sensors." Recognizing that the Spivey et al. reference does not disclose a fabrication process as recited in claim 17, the Examiner proposes to modify the reference to Spivey et al. based on the disclosure of Sayag et al. To do so, however, would be contrary to the design strategy of the Spivey et al. reference, which obtains a large-format array by locating the readout areas on edges of the single

large image sensor portion, or by integrating readout circuitry into each of the pixels. Claim 17 is not rendered obvious by the references to Spivey et al. and Sayag et al.

The references to Thevenin et al. and Heller et al., and the Examiner' official notice, do not cure the deficiencies of Spivey et al. and Sayag et al. Thevenin et al. teaches readout circuitry located underneath the pixel array. Heller et al. teaches readout circuitry separated completely from the imager array. The Examiner's official notice relates to providing thin edges in imaging devices. None of these references can provide motivation to modify the teachings of Spivey et al. based on Sayag et al.

Claim 17, and its dependent claim 18, are submitted as patentable over the references to Spivey et al., Sayag et al., Thevenin et al., and Heller et al., and the Examiner's official notice.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Spivey et al. in view of Sayag et al, further in view of Thevenin et al. This rejection respectfully is traversed.

Claim 13 recites a CMOS image sensor circuit having "a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first area and a second area." The "first CMOS image sensor substrate" is formed to have "at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge." The first CMOS image sensor substrate extends "between said first edge, said second edge, and said third edge, such that said first area of said image sensor portion is adjacent said first edge and said third edge of said image sensor substrate and said second area of said image sensor portion is adjacent said second edge and said third edge of said first CMOS image sensor

substrate." The row logic is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion." A pixel interpolator and the chip driver circuitry are "located between said first portion and said second portion of said image sensor portion and said fourth edge of said image sensor substrate." "A second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate" is "abutted to one of said edges of said first CMOS image sensor substrate."

The reference to Spivey et al. teaches a CMOS image sensor circuit featuring an array divided into a large image portion and a small control portion. According to the design strategy disclosed by Spivey et al., the control portion is located on edges of the array, or integrated into pixels of the array, in order to obtain a large-format imager with few critical defects. The Spivey et al. reference does not teach or suggest, but instead teaches away from, a CMOS image sensor circuit in which an image sensor portion has "a first area and a second area," and row logic is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion." Claim 13 is submitted to be patentable over the reference to Spivey et al.

The reference to Sayag et al. does not cure the deficiencies of the Spivey et al. reference. Sayag et al. teaches a CMOS imager circuit having a centrally-located photosensitive read-out register. The Examiner proposes to modify the circuit disclosed by Spivey et al. based on the disclosure of Sayag et al. The proposed modification, however, requires a reconstruction of the circuit disclosed by Spivey et al. in a manner contrary to the design strategy of the Spivey et al. reference. Claim 13 is not rendered obvious by the references to Spivey et al. and Sayag et al.

The reference to Thevenin et al. does not cure the deficiencies of the Spivey et al. and Sayag et al. references. The Thevenin et al. reference teaches locating read-out circuitry underneath a pixel array. The reference to Thevenin et al. can not provide the motivation to modify the disclosure of Spivey et al. based on the teachings of Sayag et al.

Claim 13 is submitted to be patentable over the cited references to Spivey et al., Sayag et al., and Thevenin et al.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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